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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,832	DING ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 25-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23 and 24* is/are allowed.

6)☒ Claim(s) *1-15,19-22 and 25-30* is/are rejected.

7)☒ Claim(s) *16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final office action

Response to the applicant's amendments

a) Applicants' argument with respect to original and amended claims 1-22 and 25-30 filled on 11/17/04 have been fully considered but they are not persuasive. The examiner would like to point out that this action is made final (MPEP 706.07a).

b) Claims 23 and 24 are allowed.

Response to the applicant's argument

In response to the applicant's argument that the reference fail to show certain features of applicants invention, it is noted that the features upon which applicant relies (i.e., "the address bits in row registers select a first column of memory **using multiplexers** and after the first column of memory is selected, first data bits are loaded from the first column of memory to column registers [emphasis added]" are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Note: claims 1 and 10 recites, "loading second data bits from first memory cells into the first registers, the first memory cells being in a first word line selected by first address bits in second register" **and does not state** "the address bits in row registers select a first column of memory **using multiplexers** and after the first column of memory is selected, first data bits are loaded from the first column of memory to column registers".

Applicant contends that the prior art of record (Yin et al.) teach loading new address bits each time data is loaded into memory in programming mode and each time data is read out of a

memory column for verification but do not teach the same address bits used to select the first and second memory cells.

The examiner disagrees since Yin et al. teach a structure and a method to allow the PLD to work in normal operation state and in a number of utility states and in normal operation state, the PLD performs the **configured logic function as programmed** by the user and in utility states, the PLD **can be programmed** (either to perform the same address or different address bits to select rows or word lines of a memory device), verified and tested (see abstract) which the programmable logic devices (PLDs) inherently performs the same or different address bits to select word lines of a memory device because by virtue of the fact the process of programming and verifying data according to a specified procedure is commonly used by all the programmable logic devices and the purpose or the aim of the programming and verifying data is to facilitate utilization of flexible and efficient memory configurations. Therefore, the applicants' argument although acknowledged, has not been found to be convincing.

In response to the applicant's argument that the reference fail to show certain features of applicants invention, it is noted that the features upon which applicant relies (i.e., "Yin does not disclose or suggest shifting programming data into the shift register at the same time that the verification data is shifted out" are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Note: claims 25 recites, "shifting first data into first registers, loading second data bits from first memory cells in a first word line into the first registers, loading the first data bits into second memory cells in a second word line shifting third data [emphasis added]" **and does not**

state "shifting programming data into the shift register **at the same time that the verification data** is shifted out".

1. Claims **1-15, 19-22 and 25-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yin et al. (U.S. PN: 5,970,005)

As per claims **1, 10 and 25,** Yin et al. teach or disclose a structure and a method for testing, programming and verification of a programming logic device (PLD) (see abstract). Yin et al. that the PLD device comprises an array of programmable memory cells, arranged as rows and columns, to store the configuration information (see col. 2, last paragraph). Further, Yin et al. in figure 1 and 2 teach a register group (50) includes first registers (row register) (53) and second registers (column register) (52) whereby the first and second registers coupled to a memory cell (20). Yi et al. **do not explicitly teach** or disclose loading the first data bits from the memory cells into the first registers, loading the second data bits into second memory cells and selected by first address bits. **However,** Yi et al. in figure 1 and 2 disclose group registers (50) and the memory cells (20) connected to each other for shifting and loading data (see the line between the elements 20 and 50) and further, Yi et al. teach that the PLD device includes a column address shift register and a row shift register whose length is the number of the memory cells in a column and in programming mode, the data in the row data shift register serve as programming data of the column selected by the address in the mode, the data in the row data shift register serve as row select data (see col. 3, lines 14-24 and col. 6, lines 10-49) which Yi et al. is basically teaching the same as the applicant's invention (shifting and loading data). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time

the invention was made to load data bits from a memory cell into register or from register to a memory cell wherein data bits selected by address bits. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because shifting and loading data from memory cells to registers and selected by an address bit are common practices of PLD devices.

As per claims **2,** Yi et al. teach all the subject matter claimed in claim 1 including Yi et al. in figure 1 and 2 teach a group of shift registers and an instruction register (40, 50) and a clock logic (44). Yi et al. **do not explicitly teach** storing data bits in the first and second set of latches. **However,** flip-flops or latches are known in the art are common circuit or device to switch states by applying a proper signal or combination signal to its input. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include flip-flops or latches to switch states for shifting and loading data between registers and memories. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because storing data using set of latches or flip-flops are well known features of programmable logic devices.

As per claims **3, 4 and 6,** Yi et al. teach all the subject matter claimed in claim 1 including Yi et al. in figure 1 teach that the outputs of the registers (50) are also connected to TDO (14) through multiplex switches controlled by associated instructions (see col. 6, lines 36-49).

As per claims **5,** Yi et al. teach all the subject matter claimed in claim 1 including Yi et al. in figure 1 teach a control logic (42) coupled to the group registers (40 and 50).

As per claims **7-9,** Yi teach all the subject matter claimed in claim 1 including Yi et al. teach the registers used for programming, verification and testing in the device are organized and further register (40) used to shift in the instructions and register (51) used to load and shift out the identification code permanently stored in the correspondent device to identify the device (see col. 6, lines 10-18).

As per claim **11**, Yi et al. teach all the subject matter claimed in claim 10 including Yi et al. in figure 1 teach that the outputs of the registers (50) are also connected to TDO (14) through multiplex switches controlled by associated instructions (see col. 6, lines 36-49).

As per claims **12, 13 and 22,** Yi et al. teach all the subject matter claimed in claim 10 and 19 including Yi et al. in figure 1 and 2 teach a group of shift registers and an instruction register (40, 50) and a clock logic (44). Yi et al. **do not explicitly teach** storing data bits in latches. **However,** flip-flops or latches are known in the art are common circuit or device to switch states by applying a proper signal or combination signal to its input. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include flip-flops or latches to switch states when shifting and loading data between registers and memories. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because storing data using set of latches or flip-flops are well known features of programmable logic devices.

As per claims **14 and 15,** Yi et al. teach all the subject matter claimed in claim 10 including Yi et al. in figure 1 teach a control logic (42) coupled to the registers (40 and 50) and the memory cells (20).

As per claim **19,** Yi et al. teach all the subject matter claimed in claim 1 including Yin et al. teach or disclose a structure and a method for testing, programming and verification of a programming logic device (PLD) (see abstract). Yin et al. that the PLD device comprises an array of programmable memory cells, arranged as rows and columns, to store the configuration information (see col. 2, last paragraph). Further, Yin et al. in figure 1 and 2 teach a register group (50) includes first registers (row register) (53) and second registers (column register) (52) whereby the first and second registers coupled to a memory cell (20). Furthermore, Yi et al. teach means for selecting a location of memory cells to be programmed verified and tested in programmable logic device (see claim 24).

As per claim **20,** Yi et al. teach all the subject matter claimed in claim 19 including Yi et al. teach a programmable logic device comprising bit programming for programming PLD device bit by bit and bit verification for verifying the PLD bit by bit (see claim 16).

As per claim **21,** Yi et al. teach all the subject matter claimed in claim 19 including Yi et al. teach a programmable logic device shifting column address to a column address register to select the column containing the cells to be programmed and shifting in a row data to a row data shift register to select the rows to be programmed (see claim 19).

As per claim **26,** Yi et al. teach all the subject matter claimed in claim 25 including Yi et al. teach the registers used for programming, verification and testing in the device are organized and further register (40) used to shift in the instructions and register (51) used to load and shift out the identification code permanently stored in the correspondent device t identify the device (see col. 6, lines 10-18).

As per claims **27 and 28,** Yi et al. teach all the subject matter claimed in claim 25 including Yi et al. teach means for selecting a location of memory cells to be programmed verified and tested in programmable logic device (see claim 24).

As per claim **29,** Yi et al. teach or disclose a structure and a method for testing, programming and verification of a programming logic device (PLD) (see abstract). Yin et al. that the PLD device comprises an array of programmable memory cells, arranged as rows and columns, to store the configuration information (see col. 2, last paragraph). Further, Yin et al. in figure 1 and 2 teach a register group (50) includes first registers (row register) (53) and second registers (column register) (52) whereby the first and second registers coupled to a memory cell (20). Yi et al. **do not explicitly teach** plurality of latches coupled to one of the plurality of registers. **However,** flip-flops or latches are known in the art are common circuit or device to switch states by applying a proper signal or combination signal to its input. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include flip-flops or latches to switch states for shifting and loading data between registers and memories. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because storing data using set of latches or flip-flops are well known features of programmable logic devices.

As per claim **30,** Yi et al. teach all the subject matter claimed in claim 29 including Yi et al. teach means for selecting a location of memory cells to be programmed verified and tested in programmable logic device (see claim 24).

Allowable subject matter

2. Claims **16-18,** are objected to as being dependent upon a rejected base claim but would be allowable if rewritten independent from including all of the limitation of the base claim and any intervening claims. The claimed invention comprises a second address bits stored in the first registers select the second row of the memory cells and the third row of the memory cells and the second data bits stored in the second row of the memory cells are loaded into the second registers when the second row is selected by the second address bits and the third data bits stored in the second registers are programmed into the third row of the memory cells when the third row is selected by the second address bit which the prior art do not teach or render obvious.

Claims **17 and 18,** which are directly or indirectly dependents of claim 16 are also objected.

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

3. Claims **23 and 24** have been allowed.

As per claim 23, the prior art, Yin et al. teach or disclose a structure and a method for testing, programming and verification of a programming logic device (PLD) (see abstract). Yin et al. that the PLD device comprises an array of programmable memory cells, arranged as rows and columns, to store the configuration information (see col. 2, last paragraph). Further, Yin et al. in figure 1 and 2 teach a register group (50) includes first registers (row register) (53) and second registers (column register) (52) whereby the first and second registers coupled to a memory cell (20). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious an embedded means for selecting the second row and the third row of memory cells using second address bits, means for verifying the second data programmed into

the second row of memory cells and means for programming third data into the third row of memory cells. Consequently, claim 23 is allowed over the prior art.

Claim 24, which is/are directly or indirectly dependent/s of claim 23 is also allowable over the prior art of record.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

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